Shaahin Angizi

Ph.D. Candidate

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Education

2016–present ***Ph.D.*, Electrical Engineering**,
Arizona State University (ASU), Tempe, AZ, USA ▷ Graduation date: June 2021
University of Central Florida (UCF), Orlando, FL, USA (transferred)
- **Advisor:** Dr. Deliang Fan
- **GPA:** 4.0/4.0

2012–2014 ***M.Sc.*, Computer Engineering**,
Azad University, Science and Research Branch, Tehran, Iran
- **Advisor:** Dr. Keivan Navi
- **GPA:** 19.13/20

2007–2012 ***B.Sc.*, Computer Engineering**,
Azad University, South Tehran Branch, Tehran, Iran
- **Advisor:** Dr. Ali Boroumandnia
- **GPA:** 16.75/20

Research Interests

- Accelerator Design for Big Data Applications: Deep Learning, Bioinformatics, Graph Processing, etc.
- In-Memory Computing (Circuit/Architecture/Algorithm) based on Volatile & Non-Volatile Memories
- Adaptive Learning for Collaborative In-Edge AI Computing IoT Systems
- Low Power and Area-Efficient In-Sensor Computing for IoT
- Rethinking Hardware Security Solution for Emerging Non-Volatile Memories
- Low power VLSI circuits

Academic Honors and Distinctions

2019 Outstanding Instructor performance, EEL 4362 Post-CMOS Devices and Circuits, UCF
2019 David T. & Jane M. Donaldson Memorial Scholarship Award, UCF
2019 Best Paper Award, 2019 ACM Great Lakes Symposium on VLSI (GLSVLSI), Washington, D.C., USA
2018 Best Ph.D. Research Award (1^{st} place), 2018 Ph.D. Forum at Design Automation Conference (DAC), San Francisco, CA, USA
2018 Best Paper Award, 2018 IEEE Computer Society Annual Symposium on VLSI (ISVLSI), Hong Kong, China
2018 IEEE/ACM Design Automation Conference (DAC) - Ph.D. Forum Travel Grant, San Francisco, CA, USA
2018 Paper of the month (October-December) of IEEE Transactions on Emerging Topics in Computing
2017 Best Paper Award, 2017 IEEE Computer Society Annual Symposium on VLSI (ISVLSI), Bochum, Germany
2017 Two Most Cited Articles in Elsevier's Microelectronics Journal
2017 Most Cited Article in Elsevier's Microprocessors and Microsystems
2017 Outstanding Reviewer Award of Microelectronics Journal and Microprocessors and Microsystems
2016 Doctoral Fellowship Award, UCF- Office of Research and Commercialization (ORC)
2014 Ranked 1^{st} among Graduate Students of Computer Engineering, Azad University, Iran.

Publications

Google Scholar(Citations:1526; h-index:22; i-index:42)

Research Direction Highlight

- Deep Learning Edge Accelerator: ASPDAC'18 [C17], DAC'18 [C19], ICCAD'18 [C23], TCAD'19 [J32]
- Graph Processing Accelerator: DATE'19 [C27], ICCAD'19 [C30], GLSVLSI'19 [C28], TMAG'20 [J34]
- Genome Analysis, HW/SW Co-design: DAC'19 [C29], DATE'20 [C34], DAC'20 [C35]
- Post-CMOS Device Modeling: DAC'18 [C18], IML'17 [J22], TCAD'18 [J24], TNANO'18 [J30], TMAG'18 [J28]

Conference Publications

C38 L. Yang, Z. He, S. Angizi and D. Fan, "Processing-In-Memory Accelerator for Dynamic Neural Network with Run-Time Tuning of Accuracy, Power and Latency," *33rd IEEE International System-on-Chip Conference (**SOCC**)*, September 8-11, 2020 (invited)

C37 S. Angizi, W. Zhang and D. Fan, "Exploring DNA Alignment-in-Memory Leveraging Emerging SOT-MRAM," *30th edition of the ACM Great Lakes Symposium on VLSI (**GLSVLSI**)*, Beijing, China, September 8-11, 2020 (Virtual).

C36 D. Reis, D. Gao, S. Angizi, X. Yin, D. Fan, M. Niemier, C. Zhuo and X.S. Hu,, "Modeling and Benchmarking Computing-in-Memory for Design Space Exploration," *30th edition of the ACM Great Lakes Symposium on VLSI (**GLSVLSI**)*, Beijing, China, September 8-11, 2020 (Virtual).

C35 S. Angizi, N. Ahmed Fahmi, W. Zhang and D. Fan, "PIM-Assembler: A Processing-in-Memory Platform for Genome Assembly," *IEEE/ACM Design Automation Conference (**DAC**)*, San Francisco, CA, July 19-23, 2020.

C34 S. Angizi, J. Sun, W. Zhang and D. Fan, "PIM-Aligner: A Processing-in-MRAM Platform for Biological Sequence Alignment," *Design, Automation and Test in Europe (**DATE**)*, 09-13 March 2020, ALPEXPO, Grenoble, France.

C33 L. Yang, S. Angizi, and D. Fan, "A Flexible Processing-in-Memory Accelerator for Dynamic Channel-Adaptive Deep Neural Networks," *Asia and South Pacific Design Automation Conference (**ASP-DAC**)*, Jan. 13-16, 2020, Beijing, China.

C32 S. Angizi, Z. He, D. Reis, X. S. Hu, W. Tsai, S. J. Lin and D. Fan, "Accelerating Deep Neural Networks in Processing-in-Memory Platforms: Analog or Digital Approach?," *IEEE Computer Society Annual Symposium on VLSI (**ISVLSI**)*, June 15-17, 2019, Miami, Florida, USA.

C31 S. Angizi and D. Fan, "Deep Neural Network Acceleration in Non-Volatile Memory: A Digital Approach?," *IEEE/ACM International Symposium on Nanoscale Architectures (**NANOARCH**)*, 17-19 July 2019, Qingdao, China.

C30 S. Angizi, and D. Fan, "ReDRAM: A Reconfigurable Processing-in-DRAM Platform for Accelerating Bulk Bit-Wise Operations," *IEEE/ACM International Conference on Computer Aided Design (**ICCAD**)*, 4-7 November 2019, Westminster, CO, USA.

C29 S. Angizi, J. Sun, W. Zhang and D. Fan, "AlignS: A Processing-In-Memory Accelerator for DNA Short Read Alignment Leveraging SOT-MRAM," *IEEE/ACM Design Automation Conference (**DAC**)*, June 2-6, 2019, Las Vegas, NV, USA.

C28 S. Angizi and D. Fan, "GraphiDe: A Graph Processing Accelerator leveraging In-DRAM-Computing," *ACM Great Lakes Symposium on VLSI (**GLSVLSI**)*, May 9-11, 2019, Washington, D.C., USA. (Best Paper Award)

C27 S. Angizi, J. Sun, W. Zhang and D. Fan, "GraphS: A Graph Processing Accelerator Leveraging SOT-MRAM," *Design, Automation and Test in Europe (**DATE**)*, March 25-29, 2019, Florence, Italy.

C26 S. Angizi, Z. He and D. Fan, "ParaPIM: A Parallel Processing-in-Memory Accelerator for Binary-Weight Deep Neural Networks," *Asia and South Pacific Design Automation Conference (**ASP-DAC**)*, Jan. 21-24, 2019, Tokyo, Japan.

C25 A. Roohi, S. Angizi, D. Fan and R. F. DeMara, "Processing-In-Memory Acceleration of Convolutional Neural Networks for Energy-Efficiency, and Power-Intermittency Resilience," *International Symposium on Quality Electronic Design (**ISQED**)*, Santa Clara, CA, USA, 6-7 March, 2019. (Best Paper Candidate)

C24 A. S. Rakin, S. Angizi, Z. He and D. Fan, "PIM-TGAN: A Processing-in-Memory Accelerator for Ternary Generative Adversarial Networks," *IEEE International Conference on Computer Design (**ICCD**)*, Oct. 7-10, 2018, Orlando, FL, USA.

C23 S. Angizi, Z. He and D. Fan, "DIMA: A Depthwise CNN In-Memory Accelerator," *IEEE/ACM International Conference on Computer Aided Design (**ICCAD**)*, Nov. 5-8, 2018, San Diego, CA, USA.

C22 Z. He, S. Angizi, A. S. Rakin and D. Fan, "BD-NET: A Multiplication-less DNN with Binarized Depthwise Separable Convolution," *IEEE Computer Society Annual Symposium on VLSI (**ISVLSI**)*, July 9-11, 2018, Hong Kong, China. (Best Paper Award)

C21 Z. He, S. Angizi and D. Fan, "Accelerating Low Bit-Width Deep Convolution Neural Network in MRAM," *IEEE Computer Society Annual Symposium on VLSI (**ISVLSI**)*, July 9-11, 2018, Hong Kong, China.

C20 S. Angizi, Z. He, Y. Bai, R. F. DeMara, J. Han, M. Lin and D. Fan, "Leveraging Spintronic Devices for Efficient Approximate Logic and Stochastic Neural Network," *ACM Great Lakes Symposium on VLSI (**GLSVLSI**)*, May 23-25, 2018 Chicago, IL, USA.

C19 S. Angizi, Z. He, A. S. Rakin and D. Fan, "CMP-PIM: An Energy-Efficient Comparator-based Processing-In-Memory Neural Network Accelerator," *IEEE/ACM Design Automation Conference (**DAC**)*, June 24-28, 2018, San Francisco, CA, USA.

C18 S. Angizi, Z. He and D. Fan, "PIMA-Logic: A Novel Processing-in-Memory Architecture for Highly Flexible and Energy-Efficient Logic Computation," *IEEE/ACM Design Automation Conference (**DAC**)*, June 24-28, 2018, San Francisco, CA, USA.

C17 S. Angizi, Z. He, F. Parveen and D. Fan, "IMCE: Energy-Efficient Bit-Wise In-Memory Convolution Engine for Deep Neural Network," *Asia and South Pacific Design Automation Conference (**ASP-DAC**)*, Jan. 22-25, 2018, Jeju Island, Korea.

C16 F. Parveen, Z. He, S. Angizi and D. Fan, "HieIM: Highly Flexible In-Memory Computing using STT MRAM," *Asia and South Pacific Design Automation Conference (**ASP-DAC**)*, Jan. 22-25, 2018, Jeju Island, Korea.

C15 S. Angizi and D. Fan, "IMC: Energy-Efficient In-Memory Convolver for Accelerating Binarized Deep Neural Network," *Neuromorphic Computing Symposium: Architectures, Models, and Applications (**NCS**)*, July 17-19, 2017, Knoxville, Tennessee.

C14 D. Fan and S. Angizi, "Energy Efficient In-Memory Binary Deep Neural Network Accelerator with Dual-Mode SOT-MRAM," *IEEE International Conference on Computer Design (**ICCD**)*, Nov. 5-8, 2017, Boston, MA.

C13 Z. He, S. Angizi, and D. Fan, "Exploring STT-MRAM based In-Memory Computing Paradigm with Application of Image Edge Extraction," *IEEE International Conference on Computer Design (**ICCD**)*, Nov. 5-8, 2017, Boston, MA.

C12 F. Parveen, S. Angizi, Z. He and D. Fan, "Low Power In-Memory Computing based on Dual-Mode SOT- MRAM," *IEEE/ACM International Symposium on Low Power Electronics and Design (**ISLPED**)*, July 24-26, 2017, Taipei, Taiwan.

C11 Z. He, S. Angizi, F. Parveen and D. Fan, "High Performance and Energy-Efficient In-Memory Computing Architecture based on SOT-MRAM," *IEEE/ACM International Symposium on Nanoscale Architectures (**NANOARCH**)*, July 25- 26, 2017, Newport, USA.

C10 D. Fan, S. Angizi and Z. He, "In-Memory Computing with Spintronic Devices," *IEEE Computer Society Annual Symposium on VLSI (**ISVLSI**)*, July 3-5, 2017, Bochum, Germany (invited).

C9 S. Angizi, Z. He, F. Parveen and D. Fan, "RIMPA: A New Reconfigurable Dual-Mode In-Memory Processing Architecture with Spin Hall Effect-Driven Domain Wall Motion Device," *IEEE Computer Society Annual Symposium on VLSI (**ISVLSI**)*, July 3-5, 2017, Bochum, Germany.

C8 F. Parveen, Z. He, S. Angizi and D. Fan, "Hybrid Polymorphic Logic Gate with 5-Terminal Magnetic Domain Wall Motion Device," *IEEE Computer Society Annual Symposium on VLSI (**ISVLSI**)*, July 3-5, 2017, Bochum, Germany. (Best Paper Award)

C7 D. Fan, Z. He and S. Angizi, "Leveraging Spintronic Devices for Ultra-Low Power In-Memory Computing: Logic and Neural Network," *60th IEEE International Midwest Symposium on Circuits and Systems (**MWCAS**)*, Aug. 6-9, 2017, Boston, MA, USA (invited)

C6 F. Parveen, S. Angizi, Z. He and D. Fan, "Hybrid Polymorphic Logic Gate Using 6 Terminal Magnetic Domain Wall Motion Device," *IEEE International Symposium on Circuits & Systems (**ISCAS**)*, Baltimore, MD, USA, May 28-31, 2017.

C5 S. Angizi, Z. He, and D. Fan, "Energy Efficient In-Memory Computing Platform Based on 4-Terminal Spin Hall Effect-Driven Domain Wall Motion Devices", *27th ACM Great Lakes Symposium on VLSI (**GLSVLSI**)*, Banff, Alberta, Canada, May 10-12, 2017.

C4 Z. He, S. Angizi, F. Parveen, and D. Fan, "Leveraging Dual-Mode Magnetic Crossbar for Ultra-low Energy In-Memory Data Encryption", *27th ACM Great Lakes Symposium on VLSI (**GLSVLSI**)*, Banff, Alberta, Canada, May 10-12, 2017.

C3 S. Angizi, Z. He, R. DeMara and D. Fan, "Composite Spintronic Accuracy-Configurable Adder for Low Power Digital Signal Processing," *18th International Symposium on Quality Electronic Design (**ISQED**)*, Santa Clara, CA, USA, 13-15 March, 2017.

C2 A. M. Chabi, A. Roohi, R. F. DeMara, S. Angizi, K. Navi, and H. Khademolhosseini, "Cost-efficient QCA reversible combinational circuits based on a new reversible gate," *in Computer Architecture and Digital Systems (**CADS**), 2015 18th IEEE CSI International Symposium on*, 2015, pp. 1-6. (Best Paper Candidate)

C1 M. R. Jahangir, S. Sheikhfaal, S. Angizi, K. Navi, and F. Ahmad, Designing Nanoelectronic-compatible 8-bit Square Root Circuit by Quantum-dot Cellular Automata, *In Proceeding of The IEEE International Symposium on Nanoelectronic and Information Systems (**iNIS**)*, Indore, India, December 21st-23rd, 2015.

Peer-Reviewed Journal Publications

J35 H. Jiang, S. Angizi, D. Fan, J. Han and L. Liu "Non-Volatile Approximate Arithmetic Circuits using Scalable Hybrid Spin-CMOS Majority Gates," *IEEE Transactions on Circuits and Systems I (**TCASI**)*, IEEE, 2020

J34 S. Angizi, Z. He, A. Chen and D. Fan, "Hybrid Spin-CMOS Polymorphic Logic Gate with Application in In-Memory Computing," *IEEE Transactions on Magnetics (**TMAG**)*, IEEE, Vol. 56, No. 2, 2020.

J33 A. Roohi, S. Angizi, S. Sheikhfaal, D. Fan and R. F. DeMara, "ApGAN: Approximate GAN for Robust Low Energy Learning from Imprecise Components," *IEEE Transactions on Computers (**TC**)*, IEEE, Vol. 69, No. 3, March 2020.

J32 S. Angizi, Z. He, A. Awad and D. Fan, "MRIMA: An MRAM-based In-Memory Accelerator," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (**TCAD**)*, IEEE, Vol. 39, No. 5, 2020.

J31 L.Yang, Z. He, S. Angizi, A. S. Rakin and D. Fan, "Sparse BD-Net: A Multiplication-Less DNN with Sparse Binarized Depth-wise Separable Convolution," *ACM Journal on Emerging Technologies in Computing Systems (**JETC**)*, Vol. 16, No. 2, 2019.

J30 S. Angizi, H. Jiang, R. F. Demara, J. Han and D. Fan, "Majority-Based Spin-CMOS Primitives for Approximate Computing," *IEEE Transactions on Nanotechnology (**TNANO**)*, IEEE, Vol. 17, No. 4, pp. 795-806, 2018.

J29 Z. He, Y. Zhang, S. Angizi, B. Gong and D. Fan, "Exploring A SOT-MRAM based In-Memory Computing for Data Processing," *IEEE Transactions on Multi-Scale Computing Systems (**TMSCS**)*, IEEE, Vol. 4, No. 4, pp. 676-685, 2018.

J28 F. Parveen, S. Angizi, Z. He and D. Fan, "IMCS2: Novel Device-to-Architecture Co-design for Low Power In-memory Computing Platform using Coterminous Spin-Switch," *IEEE Transactions on Magnetics (**TMAG**)*, IEEE, Vol. 54, No. 7, 2018.

J27 F. Parveen, S. Angizi and D. Fan, " IMFlexCom: Energy Efficient In-memory Flexible Computing using Dual-mode SOT-MRAM," *ACM Journal on Emerging Technologies in Computing Systems (**JETC**)*, ACM, Vol. 14, No. 3, 2018.

J26 S. Azimi, S. Angizi and M. H. Moaiyeri, "Efficient and Robust SRAM Cell Design Based on Quantum-Dot Cellular Automata," *ECS Journal of Solid State Science and Technology*, IOP Science, Vol. 7, No.3, pp. Q38-Q45, 2018.

J25 H. Khademolhosseini, S. Angizi and Y. Nemati, "A Fault-Tolerant Design for 3-Input Majority Gate in Quantum-Dot Cellular Automata," *Journal of Nanoelectronics and Optoelectronics*, ASP, Vol. 13, No. 1, 2018.

J24 S. Angizi, Z. He, N. Bagherzadeh and D. Fan, "Design and Evaluation of a Spintronic In-Memory Processing Platform for Non-Volatile Data Encryption," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (**TCAD**)*, IEEE, Vol. 37, No.9, pp. 1788-1801, 2018.

J23 M. H. Moaiyeri, F. Sabetzadeh, and S. Angizi, "An efficient majority-based compressor for approximate computing in the nano era," *Microsystem Technologies*, Springer, Vol. 24, No. 3, pp. 1589–1601, 2017.

J22 Z. He, S. Angizi, and D. Fan, "Current Induced Dynamics of Multiple Skyrmions with Domain Wall Pair and Skyrmion-based Majority gate Design", *IEEE Magnetics Letters (**IML**)*, IEEE, Vol. 8, March 30, 2017.

J21 E. Taherkhani, M. H. Moaiyeri, and S. Angizi, "Design of an Ultra-Efficient Reversible Full Adder-Subtractor in Quantum-dot Cellular Automata," *Optik-International Journal for Light and Electron Optics*, Elsevier, Vol. 142, August 2017, pp. 557-563, 2017.

J20 M. B. Khosroshahy, M. H. Moaiyeri, S. Angizi, N. Bagherzadeh, and K. Navi, "Quantum-Dot Cellular Automata Circuits with Reduced External Fixed Inputs," *Microprocessors and Microsystems*, Elsevier, Vol. 50, May 2017, pp. 154-163, 2017.

J19 Z. Rouhani, S. Angizi, M. Taheri, K. Navi, and N. Bagherzadeh, "Towards Approximate Computing with Quantum-Dot Cellular Automata," *Journal of Low Power Electronics*, ASP, Vol. 13, No. 1, pp. 29-35, 2017.

J18 A. M. Chabi, A. Roohi, H. Khademolhosseini, S. Sheikhfaal, S. Angizi, K. Navi, and R. F. DeMara, "Towards ultra-efficient QCA reversible circuits," *Microprocessors and Microsystems*, Vol. 49, pp. 127-138, 2017.

J17 A. Roohi, R. Zand, S. Angizi, and R. F. DeMara, "A Parity-Preserving Reversible QCA Gate with Self-Checking Cascadable Resiliency", *IEEE Transactions on Emerging Topics in Computing (**TETC**)*, IEEE, Vol. 6, No. 4, pp. 450 - 459, 2018. (Featured Paper)

J16 K. Navi, S. Khammar, S. Angizi, S. Sheikhfaal, and S. Angizi, "Excess Electron Quantum-Dot Cellular Automata Cell," *Quantum Matter*, ASP, Vol. 5, no. 1, pp. 188-190, 2016.

J15 F. Ahmad, G. M. Bhat, H. Khademolhosseini, S. Azimi, S. Angizi, and K. Navi, "Towards single layer quantum- dot cellular automata adders based on explicit interaction of cells", *Journal of Computational Science*, Elsevier, Vol. 16, No. September 2016, pp. 8-15, 2016.

J14 S. Sarmadi, S. Sayedsalehi, M. Fartash, and S. Angizi, "A structured ultra-dense QCA one-bit full-adder cell", *Quantum Matter*, ASP, Vol. 5, No. 1, pp. 118-123, 2016.

J13 S. Angizi, M. H. Moaiyeri, S. Farrokhi, K. Navi, and N. Bagherzadeh, "Designing Quantum-dot Cellular Automata Counters with Energy Consumption Analysis", *Microprocessors and Microsystems*, Elsevier, Vol. 39, No. 7, pp. 512-520, 2015. (Most Cited Article)

J12 S. Angizi, S. Sayedsalehi, A. Roohi, N. Bagherzadeh, and K. Navi, "Design and verification of new n-bit quantum-dot synchronous counters using majority function-based JK flip-flops", *Journal of Circuits, Systems, and Computers*, World Scientific, Vol. 24, No. 10, pp. 1-17, 2015.

J11 S. Angizi, S. Sarmadi, S. Sayedsalehi, and K. Navi, "Design and evaluation of new majority gate-based RAM cell in quantum-dot cellular automata", *Microelectronics Journal*, Elsevier, Vol. 46, No. 1, pp. 43-51, 2015. (Most Cited Article)

J10 S. Sheikhfaal, S. Angizi, S. Sarmadi, M. H. Moaiyeri, and S. Sayedsalehi, "Designing efficient QCA logical circuits with power dissipation analysis", *Microelectronics Journal*, Elsevier, Vol. 46, No. 6, pp. 462–471, 2015. (Most Cited Article)

J9 S. Angizi, F. Danehdaran, S. Sarmadi, S. Sheikhfaal, N. Bagherzadeh, and K. Navi, "An Ultra-high Speed and Low Complexity QCA Full Adder", *Journal of Low Power Electronics*, ASP, Vol. 11, No. 2, pp. 173-180, 2015.

J8 S. Sayedsalehi, M. Rahimi Azghadi, S. Angizi, and K. Navi, "Restoring and Non-Restoring Array Divider Designs in Quantum-dot Cellular Automata", *Information sciences*, Elsevier, Vol. 311, pp. 86-101, 2015.

J7 S. Mohammadyan, S. Angizi, and K. Navi, "New fully single layer QCA full-adder cell based on feedback model", *Int. J. of High Performance Systems Architecture*, Inderscience, Vol. 5, No. 4, pp. 202 - 208, 2015.

J6 K. Navi, H. Mohammadi, and S. Angizi, "A Novel Quantum-dot Cellular Automata Reconfigurable Majority Gate with 5 and 7 Inputs Support", *Journal of Computational and Theoretical Nanoscience*, ASP, Vol. 12, No. 3, pp. 399-406, 2015.

J5 S. Sheikhfaal, K. Navi, S. Angizi, and A. Habibizad Navin, "Designing High Speed Sequential Circuits by Quantum-Dot Cellular Automata: Memory Cell and Counter Study", *Quantum Matter*, ASP, Vol. 4, No. 2, pp. 190-197, 2015.

J4 S. Sarmadi, S. Azimi, S. Sheikhfaal, S. Angizi, "Designing Counter Using Inherent Capability of Quantum-dot Cellular Automata Loops", *International Journal of Modern Education & Computer Science*, Vol. 7, No. 9, pp. 22-28, 2015.

J3 S. Angizi, E. Alkaldy, N. Bagherzadeh, and K. Navi, "Novel Robust Single Layer Wire Crossing Approach for Exclusive OR Sum of Products Logic Design with Quantum-Dot Cellular Automata", *Journal of Low Power Electronics*, ASP, Vol. 10, No. 2, pp. 259-271, 2014.

J2 S. Angizi, K. Navi, S. Sayedsalehi, and A. Habibizad Navin, "Efficient Quantum Dot Cellular Automata Memory Architectures Based on the New Wiring Approach", *Journal of Computational and Theoretical Nanoscience*, ASP, Vol. 11, No. 11, pp. 2318-2328, 2014.

J1 A. M. Chabi, S. Sayedsalehi, S. Angizi, and K. Navi, "Efficient QCA Exclusive-or and Multiplexer Circuits Based on a Nanoelectronic-compatible Designing Approach", *International Scholarly Research Notices*, Hindawi, Volume 2014, Article ID 463967, pp. 1-9, 2014.

Professional Service

I. Research Assistant

2020-present **Research Assistant**, School of Electrical, Computer and Energy Engineering, Arizona State University, Tempe, AZ

2016-2020 **Research Assistant**, Department of Electrical and Computer Engineering, University of Central Florida, Orlando, FL

2012-2016 **Senior Research Assistant**, School of Computer Science, Institute for Research in Fundamental Sciences (IPM), Tehran, Iran

II. Teaching Experiences

Fall 2019 **Primary Instructor**, EEL 4362: Post-CMOS Devices and Circuits, Undergraduate Course, University of Central Florida, Orlando, FL

Fall 2015 **Teaching Assistant**, Computer Engineering Seminar, SBU, G. C., Tehran, Iran

Spring 2015 **Teaching Assistant**, Nanotechnology and Quantum Computing/ Computer Architecture, Azad University, Science and Research Branch, Tehran, Iran

Spring 2014 & Fall 2014 **Teaching Assistant**, Digital Logic Design/ Computer Organization, Azad University, South Tehran Branch, Tehran, Iran

Fall 2013 **Teaching Assistant**, Advanced VLSI, Azad University, Science and Research Branch, Tehran, Iran

Spring 2013 **Teaching Assistant**, Advanced Computer Architecture, Teaching Assistant, Azad University, Science and Research Branch, Tabriz, Iran

III. Reviewer

- IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD)
- IEEE Transactions on Nanotechnology (TNANO)
- IEEE Transactions on Emerging Topics in Computing (TETC)
- IEEE Transactions on VLSI (TVLSI)
- IEEE Transactions on Circuits and Systems I (TCASI) and Express Briefs (TCASII)
- IEEE Transactions on Computers (TC)
- IEEE Transactions on Magnetics (TMAG)
- ACM Journal on Emerging Technologies in Computing Systems (JETC)
- IET Micro & Nano Letters/ IET Quantum Communication/ IET Circuits, Devices & Systems
- Elsevier Integration, the VLSI Journal/ Elsevier Physica B: Condensed Matter/ Elsevier Microelectronics Journal/ Elsevier Microprocessors and Microsystems/ Elsevier Computers & Electrical Engineering
- Journal of Circuits, Systems, and Computers
- DAC/ICCAD/ASP-DAC/DATE/Micro/HPCA/ISVLSI/ISCAS/GLSVLSI/ISLPED/ISQED/...

IV. Contribution on Funded Proposals

2018 Active Collaboration in a funded National Science Foundation (NSF) project: FET: Small: "AlignMEM: Fast and Efficient DNA Sequence Alignment in Non-Volatile Magnetic RAM", 2019-2022.

2016 Active Collaboration in a funded National Science Foundation (NSF): E2CDA/ SRC project: "Non-Volatile In-Memory Processing Unit: Memory, In-Memory Logic and Deep Neural Network", 2017-2020.

Technical Skills

- Programming: *Python/C#/ C++/C/Matlab.*
- HDL Programming: *VHDL/ Verilog.*
- Parallel Programming: *Pthread/ CUDA.*
- Device level tools: *OOMMF/ mumax3.*
- Circuit level tools: *HSPICE/ Cadance Virtuoso/ SoC Encounter/ Design Compiler/ Modelsim/ Berkeley's ABC/ Xilinx ISE/ Proteus/ QCADesigner/ QCAPro/ HDLQ.*
- Architectural level tools: *Cacti/ NVsim/ NVmain/ Simple Scaler/ gem5.*
- Deep learning tools: *Tensor Flow/ Torch.*

Selected Research Presentations

P8 "A Processing-in-MRAM Accelerator for DNA Alignment and Assembly," ***SRC TECHCON***, Virtual, 2020.

P7 "Exploring DNA Alignment-in-Memory Leveraging Emerging SOT-MRAM," *30th edition of the ACM Great Lakes Symposium on VLSI (**GLSVLSI**)*, Beijing, China, September 8-11, 2020.

P6 "AlignS: A Processing-In-Memory Accelerator for DNA Short Read Alignment Leveraging SOT-MRAM," *IEEE/ACM Design Automation Conference (**DAC**)*, June 2-6, 2019, Las Vegas, NV, USA.

P5 "GraphiDe: A Graph Processing Accelerator leveraging In-DRAM-Computing," *ACM Great Lakes Symposium on VLSI (**GLSVLSI**)*, May 9-11, 2019, Washington, D.C., USA. **(Best Paper Award)**

P4 "CMP-PIM: An Energy-Efficient Comparator-based Processing-In-Memory Neural Network Accelerator," *IEEE/ACM Design Automation Conference (**DAC**)*, June 24-28, 2018, San Francisco, CA, USA.

P3 "PIM-TGAN: A Processing-in-Memory Accelerator for Ternary Generative Adversarial Networks," *IEEE International Conference on Computer Design (**ICCD**)*, Oct. 7-10, 2018, Orlando, FL, USA.

P2 "Design and Evaluation of Reconfigurable Processing-in-Memory Accelerators for Non-volatile Bit-wise Operations and Deep Learning," *IEEE/ACM Design Automation Conference (**DAC**)* PhD Forum, June 24-28, 2018, San Francisco, CA, USA. **(Best Poster Award)**

P1 "PIMA-Logic: A Novel Processing-in-Memory Architecture for Highly Flexible and Energy-Efficient Logic Computation," *IEEE/ACM Design Automation Conference (**DAC**)*, June 24-28, 2018, San Francisco, CA, USA.

References

- **Dr. Deliang Fan**
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- **Dr. Xiaobo Sharon Hu**
  Professor, IEEE Fellow – University of Notre Dame, IN
  Email: shu@nd.edu Tel.: (574) 631-6015 Website
- **Dr. Jae-sun Seo**
  Associate Professor – Arizona State University, AZ
  Email: jaesun.seo@asu.edu Tel.: (480) 727-2660 Website
- **Dr. Amro Awad**
  Assistant Professor – North Carolina State University, NC
  Email: ajawad@ncsu.edu Tel.: (919) 515-5257 Website

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